We Claim:

1. A method for writing and reading data from a dynamic memory circuit, the dynamic memory circuit having memory cells addressed by word lines and bit lines, a word line being activated in an event of addressing of a memory area with a specific address, each of the word lines having a plurality of mutually separate word line sections, and via the bit lines, in the event of addressing with the specific address, in parallel, a number of data being able to be written to the memory cells addressed by the address or the data being able to be read from the memory cells addressed by the address, which comprises the step of:

activating only a portion of the word line sections in the event of addressing with the specific address, resulting in only a portion of the memory cells being addressed by the word line and being written to in parallel or read from in parallel.

2. The method according to claim 1, which further comprises carrying out an activation of only a portion of the word lines if, at a same time, only a second number of the data, which is less than a first number of the data, are intended to be written to the memory cells addressed by the address or to be read from the memory cells addressed by the address.

3. The method according to claim 1, which further comprises writing-in in parallel or reading-out in parallel eight bits of data in the event of addressing of the word line with an address.

4. The method according to claim 1, which further comprises writing-in or reading-out the data to/from the memory cells in the event of a rising and a falling edge.

5. A circuit for writing and reading data from a dynamic integrated memory circuit, the dynamic integrated memory circuit having memory cells addressed by word lines and bit lines, a word line being activated in an event of addressing with a specific address, the word line having a plurality of mutually separate word line sections, via the bit lines, in the event of addressing with the specific address, in parallel, a first number of data being able to be written to memory cells addressed by the addressing or being able to be read from the memory cells addressed by the address, the circuit comprising:

a drive circuit for activating only a portion of the word line sections in the event of addressing with the specific address, so that only a portion of the memory cells connected to the word line can be written to in parallel or read from in parallel.

6. The circuit according to claim 5, wherein said drive circuit activates only a portion of the word line sections or all the word line sections of the word line, in dependence on a control signal.

7. The circuit according to claim 6, wherein the control signal can be applied to an external terminal of the dynamic integrated memory circuit, the external terminal being a control terminal of the dynamic integrated memory circuit.

8. The circuit according to claim 5, wherein each of the word lines has two of the word line sections.

9. An integrated memory circuit, comprising:

word lines having a plurality of mutually separate word line sections;

bit lines;

memory cells connected to and addressed by said word lines and said bit lines, a word line being activated in an event of addressing with a specific address, and through said bit lines, in the event of addressing with the specific address, in parallel, a first number of data being able to be written

to said memory cells addressed by the addressing or being able to be read from said memory cells addressed by the address; and

a drive circuit connected to said word lines and activating only a portion of said word line sections in the event of addressing with the specific address, so that only a portion of said memory cells connected to said word line can be written to in parallel or read from in parallel.

10. A method for writing and reading data from a dynamic memory circuit, the dynamic memory circuit having memory cells addressed by word lines and bit lines, a word line being activated in an event of addressing of a memory area with a specific address, each of the word lines having a plurality of mutually separate word line sections, and via the bit lines, in the event of addressing with the specific address, in parallel, a number of data being able to be written to the memory cells addressed by the address or the data being able to be read from the memory cells addressed by the address, which comprises the step of:

applying a control signal to a control terminal of the integrated memory for activating only a portion of the word line sections in the event of addressing with the specific address, resulting in only a portion of the memory cells being

addressed by the word line and being written to in parallel or read from in parallel.

11. The method according to claim 10, which further comprises using a terminal of the integrated memory that is not an address terminal or a data terminal as the control terminal.